S/N 09/256643 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Michael Trinh
Serial No.:	09/256643	Group Art Unit:	2822
Filed:	February 23, 1999	Docket:	303.324US2
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE		

INFORMATION DISCLOSURE STATEMENT

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6973

Date 8 December 2003

By _____
Robert E. Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE; Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of December, 2003.

Amy Moriarty
Name

_____
Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	09/256643
Filing Date	February 23, 1999
First Named Inventor	Forbes, Leonard
Group Art Unit	2822
Examiner Name	Trinh, Michael
Attorney Docket No: 303.324US2	

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,598,305	07/01/1986	Chiang, A. , et al.	357	23.7	06/18/1984
	US-4,736,317	04/05/1988	Hu, M. , et al.	364	200	07/17/1985
	US-4,816,883	03/28/1989	Baldi, Livio	357	23.5	06/22/1987
	US-4,980,303	12/25/1990	Yamauchi, T.	437	31	08/18/1988
	US-4,994,401	02/19/1991	Ukai, Y.	437	40	03/26/1990
	US-5,189,504	02/23/1993	Nakayama, S. , et al.	257	422	01/30/1992
	US-5,317,535	05/31/1994	Talreja, Sanjay S., et al.	365	185	06/19/1992
	US-5,336,361	08/09/1994	Tamura, A. , et al.	438	767	11/02/1992
	US-5,367,306	11/22/1994	Hollon, , et al.	342	386	06/04/1993
	US-5,388,069	02/07/1995	Kokubo, Masaya	365	185	03/18/1993
	US-5,409,501	04/25/1995	Zauns-Huber, R. , et al.	8	94.29	07/06/1992
	US-5,424,993	06/13/1995	Lee, Roger R., et al.	365	218	11/15/1993
	US-5,438,544	08/01/1995	Makino, Takami	365	185	01/28/1994
	US-5,467,306	11/14/1995	Kaya, Cetin , et al.	365	185.2	10/04/1993
	US-5,493,140	02/20/1996	Iguchi, Katsuji	257	316	06/21/1994
	US-5,912,837	06/15/1999	Lakhani,	365	185.02	10/28/1996
	US-5,990,531	11/23/1999	Taskar, N. R., et al.	257	410	11/12/1997
	US-6,031,263	02/29/2000	Forbes, L. , et al.	257	315	07/29/1997
	US-6,100,193	08/08/2000	Suehiro, S. , et al.	438	685	09/24/1997
	US-6,166,768	12/26/2000	Fossum, , et al.	348	308	01/22/1997
	US-6,365,919	04/02/2002	Tihanyi, J. , et al.	257	77	07/11/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]
	JP-08-255878	10/01/1996	Sugita, Y	H01L	27/10	
	JP-60-024678	02/07/1985	Akio, Nakatani	G06 K	9/36	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		BOERINGER, DANIEL W., et al., "Avalanche amplificaiton of multiple resonant tunneling through parallel silicon microcrystallites", Physical Rev. B, 51, (1995),13337-13343	
		BURNS, S. G., et al., In: Principles of Electronic Circuits, West Publishing Co., St. Paul, MN,(1987),382-383	

EXAMINER **DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	09/256643
Filing Date	February 23, 1999
First Named Inventor	Forbes, Leonard
Group Art Unit	2822
Examiner Name	Trinh, Michael

Sheet 2 of 2

Attorney Docket No: 303.324US2

		EDELBERG, E. , et al., "Visible Luminescence from Nanocrystalline silicon films produced by plasma enhanced chemical vapor deposition", Appl. Phys. Lett., 68, (1996),1415-1417	
		HYBERTSEN, MARK S., "Absorption and Emission of Light in Nanoscale Silicon Structures", Phys. Rev. Lett., 72, (1994),1514-1517	
		KATO, MASATAKA , et al., "Read-Disturb Degradation Mechanism due to Electron Trapping in the Tunnel Oxide for Low-voltage Flash Memories", IEEE Electron Device Meeting, (1994),45-48	
		NAKAMURA, J. , et al., "CMOS Active Pixel Image Sensor with Simple Floating Gate Pixels", IEEE Transactions on Electron Devices, 42, (1995),1693-1694	
		RUSKA, W. S., "Microelectronic Processing", McGraw-Hill Book Co., (1987),281	
		SCHOENFELD, O. , et al., "Formation of Si Quantum dots in Nanocrystalline silicon", Proc. 7th Int. Conf. on Modulated Semiconductor Structures, Madrid, (1995),605-608	
		TSU, RAPHAEL , et al., "Slow Conductance oscillations in nanoscale silicon clusters of quantum dots", Appl. Phys. Lett., 65, (1994),842-844	
		WOLF, S. , Silicon Processing for the VLSI Era, Vol. 3, Lattice Press, Sunset Beach, CA,(1995),311-312	
		YE, QIU-YI , et al., "Resonant Tunneling via Microcrystalline-silicon quantum confinement", Physical Rev. B, 44, (1991),1806-1811	
		ZHAO, X. , et al., "Nanocrystalline Si: a material constructed by Si quantum dots", 1st Int. Conf. on Low Dimensional Structures and Devices, Singapore, (1995),467-471	

EXAMINER **DATE CONSIDERED**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Michael Trinh
Serial No.:	09/256643	Group Art Unit: 2822
Filed:	February 23, 1999	Docket: 303.324US2
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/652420	August 31, 2000	303.324US3	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
09/691004	October 18, 2000	303.324US4	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
08/903486	July 29, 1997	303.326US1	SILICON CARBIDE GATE TRANSISTOR
09/259870	March 1, 1999	303.326US2	FABRICATION OF SILICON CARBIDE GATE TRANSISTOR
08/902132 5886368	July 29, 1997	303.353US1	TRANSISTOR WITH SILICON OXYCARBIDE GATE AND METHODS OF FABRICATION AND USE
09/138294 6309907	August 21, 1998	303.353US2	TRANSISTOR WITH SILICON OXYCARBIDE GATE AND METHODS OF FABRICATION AND USE
08/902843	July 29, 1997	303.354US1	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE

			INSULATOR
09/135413	August 14, 1998	303.354US2	METHOD FOR OPERATING A DEAPROM HAVING AN AMORPHOUS SILICON CARBIDE GATE INSULATOR
09/134713	August 14, 1998	303.354US3	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
08/902098 6031263	July 29, 1997	303.355US1	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
09/140978 6307775	August 27, 1998	303.355US2	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
09/141392 6249020	August 27, 1998	303.355US3	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
09/883795	June 18, 2001	303.355US4	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
10/047181	October 23, 2001	303.355US5	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
08/902133	July 29, 1997	303.356US1	MEMORY DEVICE
10/231687	August 29, 2002	303.356US2	DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY DEVICE
08/903453	July 29, 1997	303.378US1	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/258467	February 26, 1999	303.378US2	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

09/650553	August 30, 2000	303.378US3	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
10/461593	June 11, 2003	303.356US3	DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY DEVICE

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6973

Date 8 December 2003 By _____

Robert E. Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of December, 2003.

Name Amy Moriarty

Signature _____